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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/519,741	11/04/2005	Ludwig Dittmar	2002 P 09188 US	9239

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EXAMINER	
DINH, THU HUONG T	

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2812	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/519,741	DITTMAR ET AL.	
	Examiner	Art Unit	
	Thu-Huong Dinh	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/19/2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) *1-20 and 28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-27,29-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in responded to Amendment received on 7/19/2007. Claims 1-20 and 28 are cancelled. Claims 21, 25,27,30-31,33-34 are amended. Currently, Claims 21-27 and 29-35 are pending.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 21, 25-27, 30, and 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lucas et al. (U.S. 6,287,951 dated September 11, 2001) in view of Chen et al. (U.S. 6,720,252 filed November 13, 2002).

Lucas et al. teach the following: 1)... providing a hard mask (34) over an insulating layer (26) pattern to define a contact hole (41); forming said contact hole (41) in said insulating layer (26) (col. 6, lines 26-31 and Fig. 4); filling the contact hole (41) with an ARC layer that also overlies said patterned hard mask (34) and the insulating layer (26) (col. 5, lines 62-63, and Fig. 3); depositing and patterning a photoresist layer (38) on said ARC layer (36) (col. 6, lines 20-22); removing portions of the ARC layer (36) and portions of the hard mask (34) not covered by the photoresist layer (38) (col.6, lines 33-36 and lines 45-46) to repattern said hard mask to define a conductive line trench (61) (col. 7, lines 8-14 and Fig. 6); removing portions of the insulating layer (26) to form said conductive

line trench (61) (col. 7, lines 15-16); removing the ARC layer (36)from the contact hole (41) (col. 7, lines 10-11 and Fig. 6); and filling the contact hole (41) and said conductive line trench (61) with contact material (74)so that the filled contact hole (41) and the conductive line trench (61)are-electrically connected (col. 7, lines 55-56 and Fig. 7 and 8)(Claim 21); 2)...further comprising depositing a liner (72) on a surface of said contact hole (41) and conductive line trench (61) prior to said step of filling with contact material (col. 7, lines 55-57 and Fig. 7)(Claim 25); 3)...wherein said liner (72) is selected from the group consisting of Ti and TiN (col. 7, lines 59-60)(Claim 26,35); 4)...wherein said step of filling the contact hole (41) with contact material (74) comprising filling said contact hole with tungsten (Col. 7, lines 60-61)(Claim 27); 5)... further comprising a step of depositing a liner (72) on a surface of said contact hole (41) and conductor trench (61) prior to said step of filling (col. 7, lines 55-57 and Fig. 7)(Claim 33); 6)... providing said insulating layer (26); providing said hard mask (34) over said insulating layer (26), said hardmask patterned to form said contact hole (41); etching said contact hole (41) in said insulating layer (26) subsequent to providing said hard mask (34) (col. 6, lines 26-32 and Fig. 4); covering said insulating layer (26) with an ARC layer to fill said contact hole (21); depositing and patterning a photoresist layer (38) that covers said ARC layer (col. 6, lines 20-22); repattern said hard mask (34) subsequent to said step of covering said insulating layer (26) with said ARC layer to define said conductor trench connected to said contact hole (col. 6, lines 22-25); etching said conductor trench in said insulating layer (26) according to said re-patterned hard mask (34) (col. 6, lines 44-52 and col. 7, lines 1-9 and

Fig. 6); and filling said contact hole (41) and said conductor trench (61) with a conductive material (74) such that said conductive material in said conductor trench (61) and said contact hole are electrically connected (Fig 9)(Claim 30); 7)...wherein said step of filling said contact hole (41) and conductor trench (61) with conductive material (74) comprises filling said contact hole and conductor trench (61) with tungsten (Col. 7, lines 60-61) (Claim 34).

Lucas et al. lack the anticipation of explicitly teaching the following: 1)... filling the contact hole with an ARC layer that also overlies said patterned hard mask and the insulating layer; removing the ARC layer from the contact hole (Claim 21); 2)... covering said insulating layer with an ARC layer to fill said contact hole; depositing and patterning a photoresist layer that covers said ARC layer (Claim 30).

Chen et al. background teach the conventional dual damascene process and during the photolithographic process, light passes through a photoresist film down to the semiconductor substrate, where the light is reflected back up through the photoresist. The reflected light could interfere with the adjacent photoresist, adversely affecting the control of the critical dimension ("CD") of the manufacturing process. Referring to FIG. 2A, a bottom anti-reflective coating ("BARC") layer 110 is formed over substrate 101, and via openings 108 are filled with BARC layer 110. The thickness of BARC layer 110 across the top surface of the underlying dielectric layer 106 varies due to changes of density of via openings 108. Specifically, BARC layer 110 provided over region 102 having denser via openings is thinner compared to region 104 having less dense via

openings. Referring to FIG. 2B, a second PR layer 112 is provided over BARC layer 110. After second PR layer 112 is defined and developed, layer 112 and BARC layer 110 are etched to form a plurality of openings 114 to define trenches generated thereafter. Next, via openings 108 and trenches 116 are filled with conductive material 118 to complete the dual damascene process.

It would be obvious to one of ordinary skill in the art, at the time of invention was made, to modify the structure shown in Lucas et al. with Chen et al. background teaching with the motivation of using ARC material to suppress unintended light reflection from a reflective surface that is beneath the photoresist.

3. Claims 22-23,29, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lucas et al. (U.S. 6,287,951 dated September 11, 2001) in view of Chen et al. (U.S. 6,720,252 filed November 13, 2002) as applied to claim 21 and 30 above, and further in view of Prior Art, Gruening-Von Schwerin et al. (U.S.2004/0206722 filed April 18, 2002).

Lucas et al. and Chen et al. lack the anticipation of explicitly teaching the following: 1)... wherein said hard mask is made from polycrystalline silicon (Claim 22,29); 2)...further comprising patterning said hard mask by means of a dry etching process (Claim 23); 3)... wherein said step of repatterning said hard mask comprises etching said hard mask by means of a dry etching process (Claim 31).

Prior Art, Gruening-Von Schwerin et al. teaches a semiconductor substrate (column 2 [0024]) providing a first contact hole (K1) in an insulating

layer (column 3 [0026]); and filling the contact hole (K1) with contact material (60) (column 5 [0060]) so that the contact material is electrically connected to a line (column 4 and column 5 [0056]); wherein a hard mask (M1) that is used to pattern the contact hole (column 5 [0057]) is subsequently re-patterned (column 5 [0058]) to define a conductor line trench (70) which is connected thereto (column 5 [0062]). Preferably, the hard mask (M1) is made from polycrystalline silicon (column 4 [0055]) and further comprising patterning said hard mask by means of a dry etching process (column 5 [0059]).

It would be obvious to one of ordinary skill in the art, at the time of invention was made, to modify the structure shown in Lucas et al. and Chen et al. with Prior Art, Gruening-Von Schwerin et al. teaches of forming contact holes to a multiplicity of contact regions of components integrated in a substrate with the motivation of a possible misalignment error of the projection mask used for fabricating the auxiliary layer does not affect subsequent further patterning steps, since the auxiliary layer does not define any permanent structures.

4. Claims 24 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lucas et al. (U.S. 6,287,951 dated September 11, 2001) in view of Chen et al. (U.S. 6,720,252 filed November 13, 2002) as applied to claim 21 and 30 above, and further in view of Prior Art, Gruening-Von Schwerin et al. (U.S.2004/0206722 filed April 18, 2002) and Carey (U.S. 5,173,442 dated December 22, 1992).

Lucas et al. and Chen et al. and Prior Art, Gruening-Von Schwerin et al. teach the structure as claimed and as described in the preceding paragraphs;

however, Lucas et al. and Chen et al. and Prior Art, Gruening-Von Schwerin et al. lack anticipation only in not explicitly the teaching of: 1) ...wherein said dry etching process comprises using at least one of the group SF_6, HBr and He/O_2 (Claims 24, 32).

Carey teaches the Methods of Forming Channels and Vias in Insulating Layers. The channels extending partially through and vias extending completely through an insulation layer in an electrical interconnect such as a substrate can be formed in a relatively few steps with low cost etching and patterning techniques. In Figure 1a, a thin blanket layer of metal is sputtered over the insulation layer as polyimide layer (14) to form hard mask (16), which after conventional patterning has openings to expose via regions (20) and channel region (22) (column 3, lines 44-50). As plasma etch (24) is applied hard mask (16) etches slowly (column 3, lines 59-60) and plasma etch (24) can comprise 90% O_2 and 10% SF_6 (column 4, lines 3). While dry etching with plasma etches is the preferred method of etching, other etching methods is suitable for selectively removing material from the insulating layer (column 4, lines 42-45).

It would be obvious to one of ordinary skill in the art, at the time of invention was made, to modify the structure shown in Lucas et al. and Chen et al. and Prior Art, Gruening-Von Schwerin et al. with Carey's teaching of forming vias in an insulation layer with the motivation of reducing cost in etching and patterning techniques.

Response to Arguments

5. Applicant's arguments with respect to claims 21, 30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thu-Huong Dinh whose telephone number is 571 272-9014. The examiner can normally be reached on Monday through Friday (8:30AM-5:00PM Eastern).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571 272-1873. The

fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thd
10/5/2007

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER